

**SC-FD-ADC-180F410**

Fully Differential 13-bit ADC

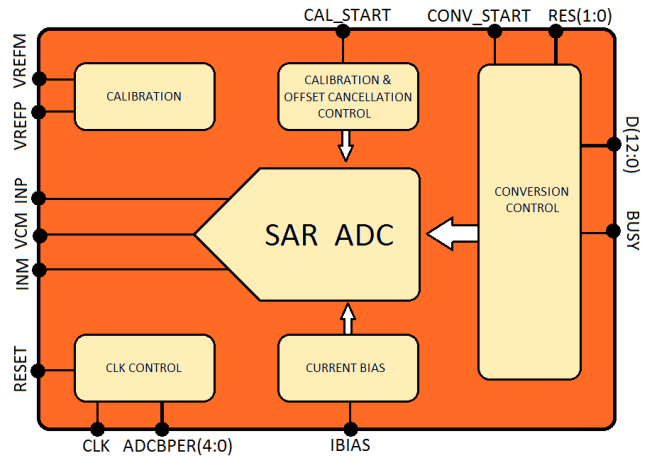
*The path from the real world to the digital word*

The **SC-FD-ADC-180F410** is a silicon **IP module** for analogue-to-digital conversion of fully differential input signal. It provides conversion with the programmable resolution, from 7 to 12 bit, with additional polarity bit. Automatic procedures for self calibration and offset cancellation are incorporated in the module to account for process imperfections and influence of the operating condition change.

As a standalone solution with interface to the digital logic, it is well suited for integration in a SoC, where solution with low power, high linearity and moderate conversion speed is needed. Conversion time is fully programmable with the resolution setting as well as with the setting of bit period. Conversion clocks are generated locally from the basic clock.

**Key Targeted Features**

- 7 to 12 bit programmable resolution with the additional polarity bit
- INL error < 0.7 LSB
- Sample speed from 27 kSPS – 7-bit to 8.5 kSPS – 13-bit
- 5 bit digital setting for bit period
- Incorporated offset cancellation procedure for internal offset
- Self calibration to set maximum input voltage range (1.3V)
- Differential input voltage range 1.3 V
- Signal ground 0.8V
- Hysteresis feature for noisy environments
- Power down mode included
- Single supply voltage: 1.6 V to 1.8 V
- Power consumption: ~ 1 mW (without digital part)
- Operating temperature range: -40°C to 125°C
- Compact IP area: ~ 0.98 mm<sup>2</sup>



**Functional block diagram SC-FD-ADC-180F410**

**Technology**

- TSMC 180nm 1P6M mixed signal

**Application Areas**

- **General purpose:** SoC or ASIC with the requirement for analogue-to-digital converter (low power, moderate speed, high linearity, compact area)
- **Integrated in SC-I-AFE-180F110:** ideally suited for the various applications (see datasheet for SC-I-AFE-180F110)

**Deliverables**

- GDSII layout database
- Behavioural VHDL model for SoC simulations
- Layout footprint
- VHDL code for synthesis

**On demand:**

- LVS/SPICE netlist
- MATLAB model for effective system design

- ❖ **SC-I-AFE-180F110** Current-Input AFE with 13-bit ADC
- ❖ **SC-IC-AFE-180F209** Current-Input AFE – Core
- ❖ **SC-I-AFE-180F210** Current-Input AFE
- ❖ **SC-IQ-IUC-180F310** Current-to-Voltage Converter
- ❖ **SC-FD-ADC-180F410** Fully Differential 13-bit ADC

**SC-IC-AFE-180F209** does not contain the block: *Digital Control & Interface* which is usually the part of overall SoC solution. This block is incorporated in **SC-I-AFE-180F210**.

**Systemcom AFE Family**

**Contact Data**

For further technical and sales communication please contact us at: [afe@systemcom.hr](mailto:afe@systemcom.hr)

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